RC5053

5-Bit Programmable Synchronous Switching Regulator Controller for Pentium® II Processor

Features

- 5-Bit Digitally Programmable 1.8V to 3.5V Fixed Output Voltage
- Provides All Features Required by the Intel Pentium II Processor VRM 8.2 DC/DC Converter Specification
- Flags for Power Good, Over-Temperature and Over-Voltage Fault
- Output Current Exceeds 14A from a 5V Supply
- Dual N-Channel MOSFET Synchronous Driver
- Initial Output Accuracy: ±1.5%
- Excellent Output Accuracy: ±2% Typ Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable Current Limit Without External Sense Resistors
- Fast Transient Response
- Available in SO-20 and SSOP-20 Packages

Applications

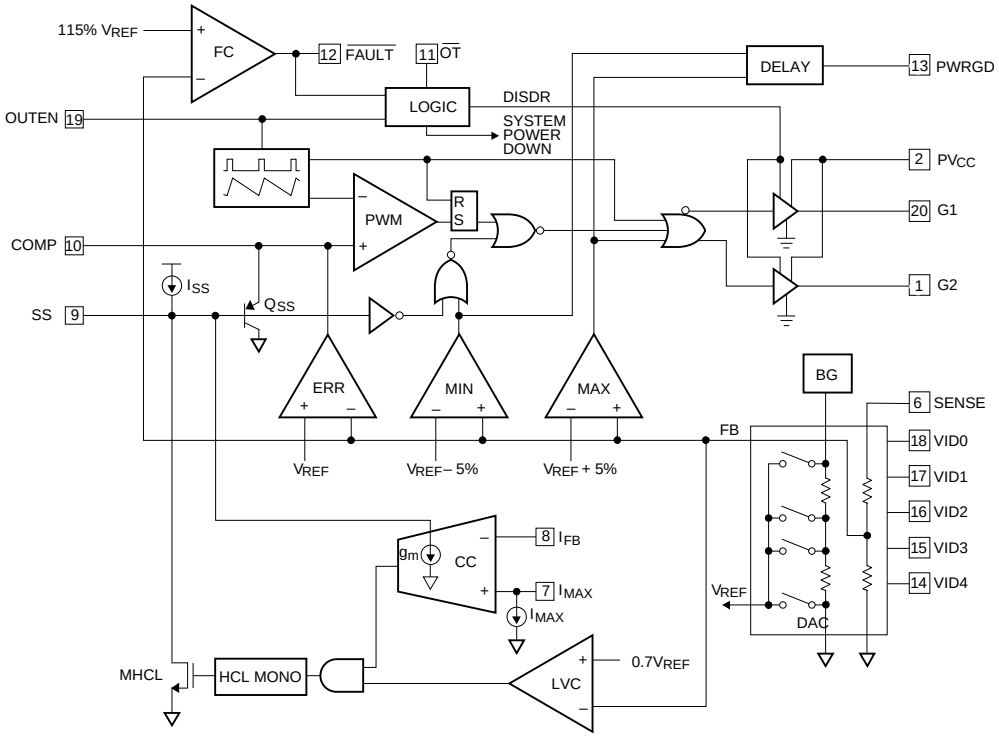
- Power Supply for Pentium II, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V to 1.8V-3.5V Regulators

Descriptions

The RC5053 is a high power, high efficiency switching regulator controller optimized for 5V input to 1.8V-3.5V output applications. It features a digitally programmable output voltage, a precision internal reference and an internal feedback system that provides output accuracy of ±1.5% at room temperature and typically ±2% over-temperature, load current and line voltage shifts. The RC5053 uses a synchronous switching architecture with two external N-channel output devices, providing high efficiency and eliminating the need for a high power, high cost P-channel device. Additionally, it senses the output current across the on-resistance of the upper N-channel MOSFET, providing an adjustable current limit without an external low value sense resistor.

The RC5053 free-runs at 300kHz and can be synchronized to a faster external clock if desired. It includes all the inputs and outputs required to implement a power supply conforming to the Intel Pentium® II Processor VRM 8.2 DC/DC Converter Specification.

Block Diagram



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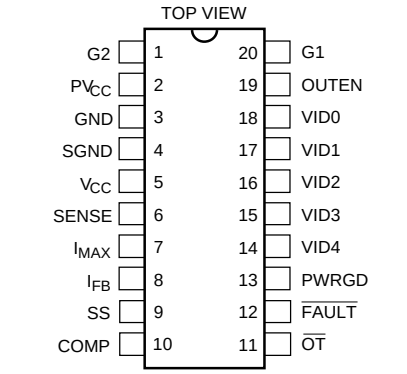
Rev. 0.9.4

Pin Assignment



F PACKAGE
20-LEAD PLASTIC SSOP

M PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (F)
T_{JMAX} = 125°C, θ_{JA} = 85.2°C/W (M)

Pin Definitions

Pin Number	Pin Name	Pin Description
1	G2	**Gate Drive for the Lower N-Channel MOSFET, Q2.** This output will swing from PV_{CC} to GND. It will always be low when G1 is high or when the output is disabled. To prevent undershoot during a soft start cycle, G2 is held low until G1 first goes high.
2	PV_{CC}	**Power Supply for G1 and G2.** PV_{CC} must be connected to a potential of at least V_{IN} + $V_{GS(ON)Q1}$. If V_{IN} = 5V, PV_{CC} can be generated using a simple charge pump connected to the switching node between Q1 and Q2 (see Figure 7), or it can be connected to an auxiliary 12V supply if one exists.
3	GND	**Power Ground.** GND should be connected to a low impedance ground plane in close proximity to the source of Q2.
4	SGND	**Signal Ground.** SGND is connected to the low power internal circuitry and should be connected to the negative terminal of the output capacitor where it returns to the ground plane. GND and SGND should be shorted right at the RC5053.
5	V_{CC}	**Power Supply.** Power for the internal low power circuitry. V_{CC} should be wired separately from the drain of Q1 if they share the same supply. A 10μF bypass capacitor is recommended from this pin to SGND.
6	SENSE	**Output Voltage Pin.** Connect to the positive terminal of the output capacitor. There is an internal 120k resistor connected from this pin to SGND. SENSE is a very sensitive pin; for optimum performance, connect an external 0.1μF capacitor from this pin to SGND. By connecting a small external resistor between the output capacitor and the SENSE pin, the initial output voltage can be raised slightly. Since the internal divider has a nominal impedance of 120kΩ, a 1200Ω series resistor will raise the nominal output voltage by 1%. If an external resistor is used, the value of the 0.1μF capacitor on the SENSE pin must be greatly reduced or loop phase margin will suffer. Set a time constant for the RC combination of approximately 0.1μs. So, for example, with a 1200Ω resistor, set C = 83pF. Use a standard 100pF capacitor.
7	I_{MAX}	**Current Limit Threshold.** Current limit is set by the voltage drop across an external resistor connected between the drain of Q1 and I_{MAX}. There is a 180μA internal pull-down at I_{MAX}.

Preliminary Information

Pin Definitions (continued)

Pin Number	Pin Name	Pin Description
8	I_{FB}	**Current Limit Sense Pin.** Connect to the switching node between the source of Q1 and the drain of Q2. If I_{FB} drops below I_{MAX} when G1 is on, the RC5053 will go into current limit. The current limit circuit can be disabled by floating I_{MAX} and shorting I_{FB} to V_{CC} through an external 10k resistor.
9	SS	**Soft Start.** Connect to an external capacitor to implement a soft start function. During moderate overload conditions, the soft start capacitor will be discharged slowly in order to reduce the duty cycle. In hard current limit, the soft start capacitor will be forced low immediately and the RC5053 will rerun a complete soft start cycle. C_{SS} must be selected such that during power-up the current through Q1 will not exceed the current limit value.
10	COMP	**External Compensation.** The COMP pin is connected directly to the output of the error amplifier and the input of the PWM comparator. An RC+ C network is used at this node to compensate the feedback loop to provide optimum transient response.
11	$\overline{OT}$	**Over-Temperature Fault.** $\overline{OT}$ is an open-drain output and will be pulled low if OUTEN is less than 2V.
12	$\overline{FAULT}$	**Overvoltage Fault.** $\overline{FAULT}$ is an open-drain output. If V_{OUT} reaches 15% above the nominal output voltage, $\overline{FAULT}$ will go low and G1 and G2 will be disabled. Once triggered, the RC5053 will remain in this state until the power supply is recycled or the OUTEN pin is toggled. If OUTEN = 0, $\overline{FAULT}$ floats or is pulled high by an external resistor.
13	PWRGD	**Power Good.** This is an open-drain signal to indicate validity of output voltage. A high indicates that the output has settled to within ±5% of the rated output for more than 1ms. PWRGD will go low if the output is out of regulation for more than 500μs. If OUTEN = 0, PWRGD pulls low.
18, 17, 16, 15, 14	VID0, VID1, VID2, VID3, VID4	**Digital Voltage Select.**TTL inputs used to set the regulated output voltage required by the processor (Table 3). There is an internal 20kΩ pull-up at each pin. When all five VIDn pins are high or floating, the chip will shut down.
19	OUTEN	**Output Enable.** TTL input which enables the output voltage.The external MOSFET temperature can be monitored with an external thermistor as shown in Figure 6. When the OUTEN input voltage drops below 2V, $\overline{OT}$ trips. As OUTEN drops below 1.7V, the drivers are internally disabled to prevent the MOSFETs from heating further. If OUTEN is less than 1.2V for longer than 30μs, the RC5053 will enter shutdown mode. The internal oscillator can be synchronized to a faster external clock by applying the external clocking signal to the OUTEN pin.
20	G1	**Gate Drive for the Upper N-Channel MOSFET, Q1.**This output will swing from PV_{CC} to GND. It will always be low when G2 is high or the output is disabled.

Absolute Maximum Ratings[1]

Parameter	Min.	Typ.	Max.
Supply Voltage			
V_{CC}			7V
PV_{CC}			13.5V
Input Voltage			
I_{FB} (Note 2)			PV_{CC} + 0.3V
I_{MAX}	-0.3V		13V
All Other Inputs	-0.3V		V_{CC} + 0.3V

Absolute Maximum Ratings[1] (continued)

Parameter	Min.	Typ.	Max.
Digital Output Voltage	-0.3V		7V
I_{FB} Input Current (Notes 2, 3)	-100mA		
Operating Temperature Range	0°C		70°C
Storage Temperature Range	-65°C		150°C
Lead Temperature (Soldering, 10 sec.)			300°C

Electrical Characteristics (V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted.)[3]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		•	4.5		5.5	V
PV_{CC}	Supply Voltage for G1, G2		•			13.2	V
V_{OUT}	1.8V Initial Output Voltage	With Respect to Rated Output Voltage (Fig. 2)			±1.5%		mV
	2.8V Initial Output Voltage				±1.5%		mV
	3.5V Initial Output Voltage				±1.5%		mV
	1.8V Initial Output Voltage		•		±2%		mV
	2.8V Initial Output Voltage		•		±2%		mV
	3.5V Initial Output Voltage		•		±2%		mV
ΔV_{OUT}	Output Load Regulation	I_{OUT} = 0 to 14A (Fig. 2)			-5		mV
	Output Line Regulation	V_{CC} = 4.75V to 5.25V (Fig. 2)			±1		mV
V_{PWRGD}	Positive Power Good Trip Point	% Above Output Voltage (Fig. 2)	•		5	7	%
	Negative Power Good Trip Point	% Below Output Voltage (Fig. 2)	•	-7	-5		%
V_{FAULT}	$\overline{FAULT}$ Trip Point	% Above Output Voltage (Fig. 2)	•	12	15	20	%
I_{CC}	Operating Supply Current	OUTEN = V_{CC} = 5V[4] (Fig. 3)	•		2.0	3.0	mA
	Shutdown Supply Current	OUTEN = 0, VID0 to VID4 Floating (Fig. 3)	•		760	1000	µA
I_{PVCC}	Supply Current	PV_{CC} = 12V, OUTEN = V_{CC}[5] (Fig. 3)			26		mA
		PV_{CC} = 12V, OUTEN = 0, VID0 to VID4 Floating			430		µA
f_{OSC}	Internal Oscillator Frequency	(Fig. 4)	•	250	300	350	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle				1.8		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle				2.8		V
G_{ERR}	Error Amplifier Open-Loop DC Gain		•	40	53		dB
g_{mERR}	Error Amplifier Transconductance		•	0.7	1.3	1.9	mmho

Preliminary Information

Electrical Characteristics (V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted.)[3] (continued)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
BW_{ERR}	Error Amplifier -3dB Bandwidth	COMP = Open			400		kHz
I_{IMAX}	I_{MAX} Sink Current	$V_{IMAX} = V_{CC}$	•	150	180	220	µA
I_{SS}	Soft Start Source Current	V_{SS} = 0.4V, V_{IMAX} = 0V, $V_{IFB} = V_{CC}$	•	-13	-10	-7	µA
I_{SSIL}	Maximum Soft Start Sink Current Under Current Limit	$V_{SENSE} = V_{OUT}$, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V[6, 7], $V_{SS} = V_{CC}$	•	30	60	150	µA
I_{SSHIL}	Soft Start Sink Current Under Hard Current Limit	V_{SENSE} = 0V, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V, $V_{SS} = V_{CC}$	•	20	45		mA
t_{SSHIL}	Hard Current Limit Hold Time	V_{SENSE} = 0V, V_{IMAX} = 4V, V_{IFB}↓ from 5V			500		µs
t_{PWRGD}	Power Good Response Time↑	V_{SENSE}↑ from 0V to Rated V_{OUT}	•	0.5	1	2	ms
t_{PWRBAD}	Power Good Response Time↓	V_{SENSE}↓ from Rated V_{OUT} to 0V	•	200	500	1000	µs
t_{FAULT}	$\overline{FAULT}$ Response Time	V_{SENSE}↑ from Rated V_{OUT} to V_{CC}	•	200	500	1000	µs
t_{OT}	$\overline{OT}$ Response Time	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	15	40	60	µs
V_{OT}	Over-Temperature Trip Point	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	1.9	2	2.12	V
V_{OTDD}	Over-Temperature Driver Disable	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	1.6	1.7	1.8	V
V_{SHDN}	Shutdown	OUTEN↓, VID0 to VID4 = 0 (Fig. 3)[8]	•	0.8	1.2	1.5	V
t_r, t_f	Driver Rise and Fall Time	(Figure 4)	•		90	150	ns
t_{NOL}	Driver Nonoverlap Time	(Figure 4)	•	30	100		ns
DC_{MAX}	Maximum G1 Duty Cycle	(Figure 4)	•	77	82	88	%
V_{IH}	VID0 to VID4 = 1 Input High Voltage		•	2			V
V_{IL}	VID0 to VID4 = 0 Input Low Voltage		•			0.8	V
R_{IN}	VID0 to VID4 = 0 Internal Pull-Up Resistance		•	10	20		kΩ
I_{SINK}	Digital Output Sink Current		•	10			mA

The • denotes specifications which apply over the full operating temperature range.

Notes:

1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
2. When I_{FB} is taken below GND, it will be clamped by an internal diode. This pin can handle input currents greater than 100mA below GND without latchup. In the positive direction, it is not clamped to V_{CC} nor PV_{CC}.
3. All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.
4. The RC5053 goes into the shutdown mode if VID0 to VID4 are floating. Due to the internal pull-up resistors, there will be an additional 0.25mA/pin if any of the VID0 to VID4 pins are pulled low.
5. Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the RC5053 operating frequency, supply voltage and the external FETs used.
6. The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.
7. Under typical soft current limit, the net soft start discharge current will be 60µA (I_{SSIL}) + [-10µA(I_{SS})] = 50µA. The soft start sink-to-source current ratio is designed to be 6:1.
8. When VID0 to VID4 are all HIGH, the RC5053 will be forced to shut down internally. The OUTEN trip voltages are guaranteed by design for all other input codes.

Typical Application

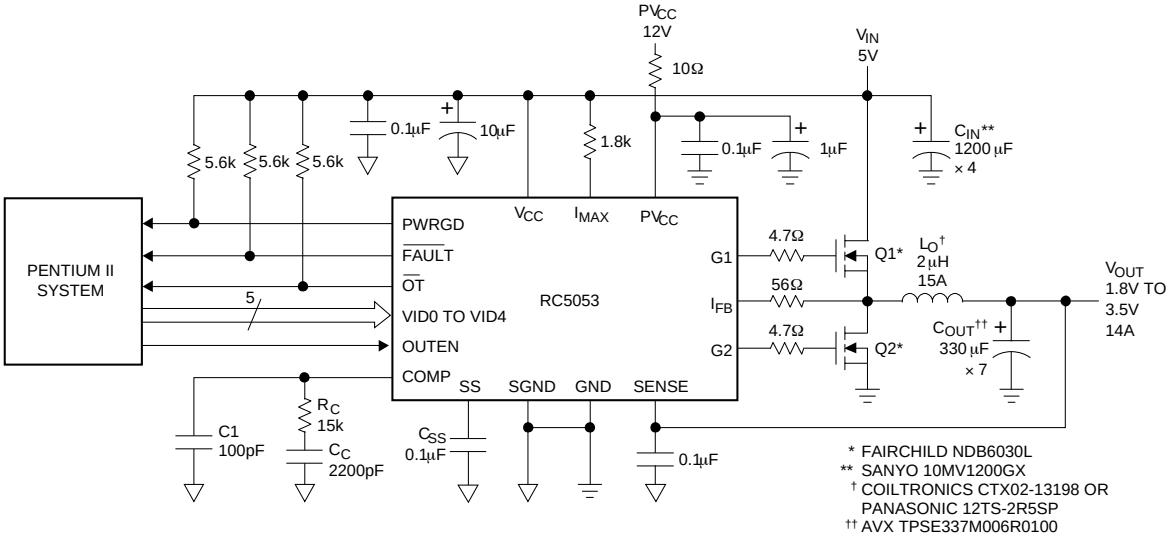


Figure 1. 5V to 1.8V-3.5V Supply Application

Test Circuits

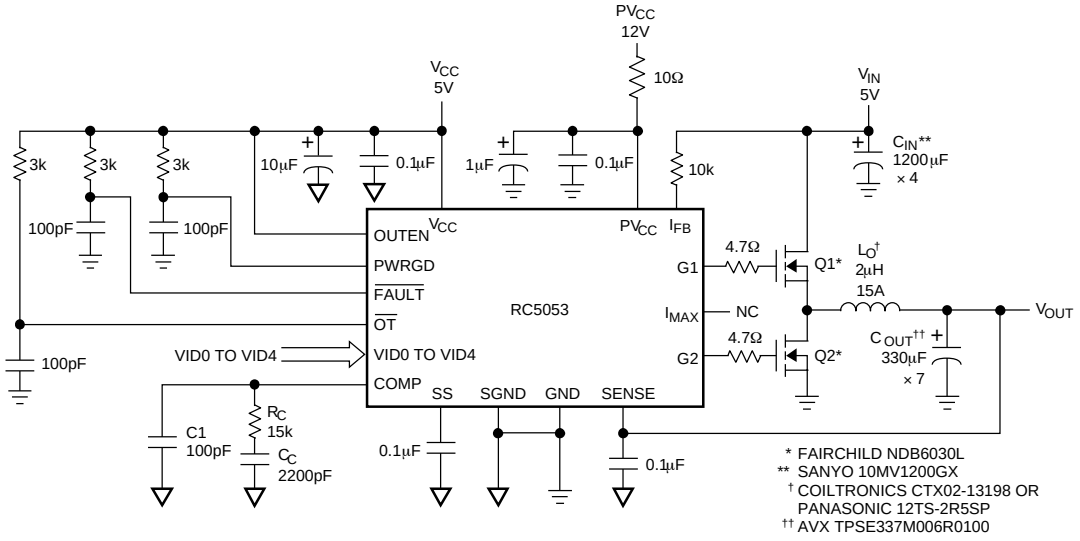


Figure 2

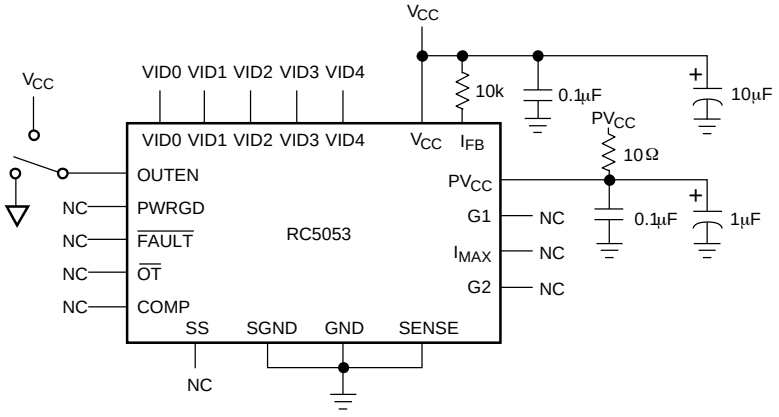


Figure 3

Test Circuits (continued)

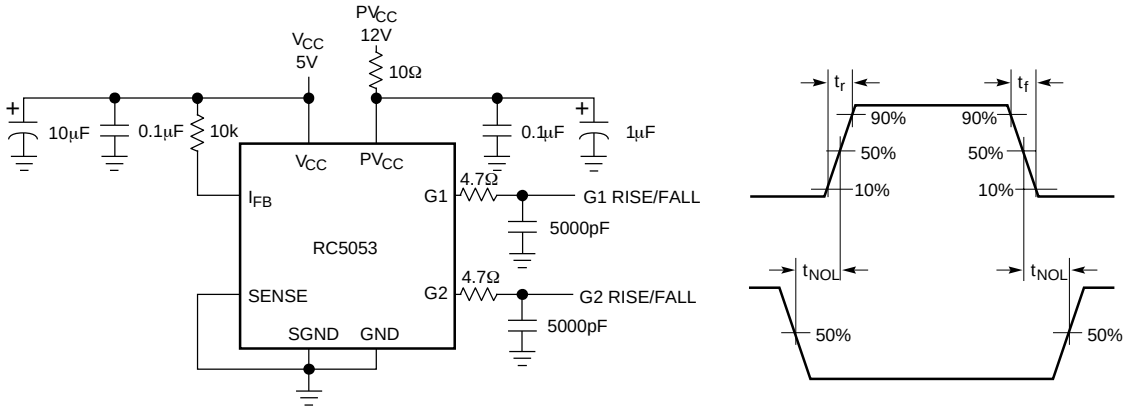


Figure 4

Function Tables

Table 1. $\overline{OT}$ Logic

OUTEN (V)	$\overline{OT}$[1]
< 2	0
> 2	1

Note:
1. With external pull-up resistor

Table 2. PWRGD and $\overline{FAULT}$ Logic

Input		Output[1]		
OUTEN	V_{SENSE}[2]	$\overline{OT}$	$\overline{FAULT}$	PWRGD
0	X	0	1	0
1	< 95%	1	1	0
1	> 95% < 105%	1	1	1
1	>105%	1	1	0
1	> 115%	1	0	0

Notes:
1. With external pull-up resistor
2. With respect to the output voltage selected in Table 3 as required by Intel Specification VRM 8.2
3. X = Don't care

Table 3. Rated Output Voltage

Input Pin					Rated Output Voltage (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	1	1	1	1	Disabled[3] (1.30)
0	1	1	1	0	Disabled[3] (1.35)
0	1	1	0	1	Disabled[3] (1.40)
0	1	1	0	0	Disabled[3] (1.45)
0	1	0	1	1	Disabled[3] (1.50)
0	1	0	1	0	Disabled[3] (1.55)
0	1	0	0	1	Disabled[3] (1.60)

Preliminary Information

Table 3. Rated Output Voltage (continued)

Input Pin					Rated Output Voltage (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	1	0	0	0	Disabled[1] (1.65)
0	0	1	1	1	Disabled[1] (1.70)
0	0	1	1	0	Disabled[1] (1.75)
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	SHDN
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Notes:
1. These code selections are disabled in RC5053

Preliminary Information

Applications Information

Overview

The RC5053 is a voltage feedback, synchronous switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It is designed to satisfy the requirements of the Intel Pentium II power supply specification. It includes an on-chip DAC to control the output voltage, a PWM generator, a precision reference trimmed to ±1%, two high power MOSFET gate drivers and all the necessary feedback and control circuitry to form a complete switching regulator circuit.

The RC5053 includes a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Once the current comparator, CC, detects an overcurrent condition, the duty cycle is reduced by discharging the soft start capacitor through a voltage-controlled current source. Under severe overloads or output short circuit conditions, the chip will be repeatedly forced into soft start until the short is removed, preventing the external components from being damaged. Under output over-voltage conditions, the MOSFET drivers will be disabled permanently until the chip power supply is recycled or the OUTEN pin is toggled.

OUTEN can optionally be connected to an external negative temperature coefficient (NTC) thermistor placed near the external MOSFETs or the microprocessor. Three threshold levels are provided internally. When OUTEN drops to 2V, $\overline{OT}$ will trip, issuing a warning to the external CPU. If the temperature continues to rise and the OUTEN input drops to 1.7V, the G1 and G2 pins will be forced low. If OUTEN is pulled below 1.2V, the RC5053 will go into shutdown mode, cutting the supply current to a minimum. If thermal shutdown is not required, OUTEN can be connected to a conventional TTL enable signal. The free-running 300kHz PWM frequency can be synchronized to a faster external clock

connected to OUTEN. Adjusting the oscillator frequency can add flexibility in the external component selection. See the Clock Synchronization section.

Output regulation can be monitored with the PWRGD pin which in turn monitors the internal MIN and MAX comparators. If the output is ±5% beyond the selected value for more than 500µs, the PWRGD output will be pulled low. Once the output has settled within ±5% of the selected value for more than 1ms, PWRGD will return high.

Theory of Operation

Primary Feedback Loop

The regulator output voltage at the SENSE pin is divided down internally by a resistor divider with a total resistance of approximately 120kΩ. This divided down voltage is subtracted from a reference voltage supplied by the DAC output. The resulting error voltage is amplified by the error amplifier and the output is compared to the oscillator ramp waveform by the PWM comparator. This PWM signal controls the external MOSFETs through G1 and G2. The resulting chopped waveform is filtered by L_O and C_{OUT} closing the loop. Loop frequency compensation is achieved with an external RC + C network at the COMP pin, which is connected to the output node of the transconductance amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the ERR amplifier may not respond quickly enough. MIN compares the feedback signal FB to a voltage 60mV (5%) below the internal reference. If FB is lower than the threshold of this comparator, the MIN comparator overrides the ERR amplifier and forces the loop to full duty cycle which is set by the internal oscillator typically to 82%. Similarly, the MAX comparator forces the output to 0% duty cycle if FB is more than 5% above the internal reference. To prevent these two comparators from triggering due to noise, the MIN and MAX comparators' response times are deliberately controlled so that they take two or three microseconds to respond. These two comparators help prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Soft Start and Current Limit

The RC5053 includes a soft start circuit which is used for initial start-up and during current limit operation. The SS pin requires an external capacitor to SGND with the value determined by the required soft start time. An internal 10µA current source is included to charge the external SS capacitor. During start-up, the COMP pin is clamped to a diode drop above the voltage at the SS pin. This prevents the error amplifier, ERR, from forcing the loop to maximum duty cycle. The RC5053 will begin to operate at low duty cycle as the SS pin rises above about 1.2V ($V_{COMP} \approx 1.8V$). As SS continues to rise, Q_{SS} turns off and the error amplifier begins to regulate the output.The MIN comparator is disabled when soft start is active to prevent it from overriding the soft start function.

The RC5053 includes yet another feedback loop to control operation in current limit. Just before every falling edge of G1, the current comparator, CC, samples and holds the voltage drop measured across the external MOSFET, Q1, at the I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As the peak current rises, the measured voltage across Q1 increases due to the drop across the $R_{DS(ON)}$ of Q1.When the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not affect the output voltage at all. More significant overload conditions will allow the SS pin to reach a steady state, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates an expensive discrete sense resistor that would otherwise be required. This helps minimize the number of components in the high current path. Due to switching noise and variation of $R_{DS(ON)}$, the actual current limit trip point is not highly accurate. The current limiting circuitry is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies.

For a given current limit level, the external resistor from I_{MAX} to V_{IN} can be determined by:

$$R_{IMAX} = \frac{(I_{LMAX})(R_{DS(ON)Q1})}{I_{IMAX}}$$

where,

$$\frac{\qquad\qquad\qquad\qquad\qquad\qquad}{2}$$

I_{LOAD} = Maximum load current;
I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = RC5053 oscillator frequency = 300kHz
L_O = Inductor value
$R_{DS(ON)Q1}$ = Hot on-resistance of Q1 at I_{LMAX}
I_{IMAX} = Internal 180µA sink current at I_{MAX}

Preliminary Information

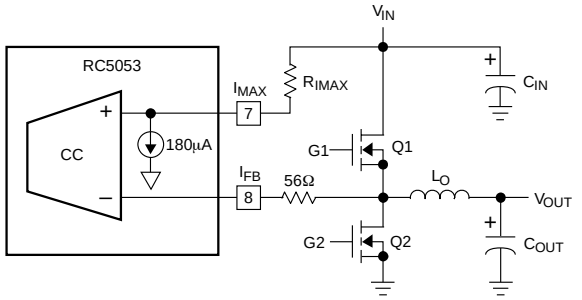


Figure 5. Current Limit Setting

OUTEN and Thermistor Input

The RC5053 includes a low power shutdown mode, controlled by the logic at the OUTEN pin. A high at OUTEN allows the part to operate normally. A low level at OUTEN stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off. $\overline{OT}$ and PWRGD are pulled low, and $\overline{FAULT}$ is left floating. In shutdown, the RC5053 quiescent current will drop to about 760µA. The remaining current is used to keep the thermistor sensing circuit at OUTEN alive. Note that the leakage current of the external MOSFETs may add to the total shutdown current consumed by the circuit, especially at elevated temperature.

OUTEN is designed with multiple thresholds to allow it to also be utilized for over-temperature protection. The power MOSFET operating temperature can be monitored with an external negative temperature coefficient (NTC) thermistor mounted next to the external MOSFET which is expected to run the hottest —often the high-side device, Q1. Electrically, the thermistor should form a voltage divider with another resistor, R1, connected to V_{CC}. Their midpoint should be connected to OUTEN (see Figure 6). As the temperature increases, the OUTEN pin voltage is reduced. Under normal operating conditions, the OUTEN pin should stay above 2V. All circuits will function normally, and the $\overline{OT}$ pin will remain in a high state. If the temperature gets abnormally high, the OUTEN pin voltage will eventually drop below 2V. $\overline{OT}$ will switch to a logic low, providing an over-temperature warning to the system. As OUTEN drops below 1.7V, the RC5053 disables both FET drivers. If OUTEN is less than 1.2V, the RC5053 will enter shutdown mode. To activate any of these three modes, the OUTEN voltage must drop below the respective threshold for longer than 30µs.

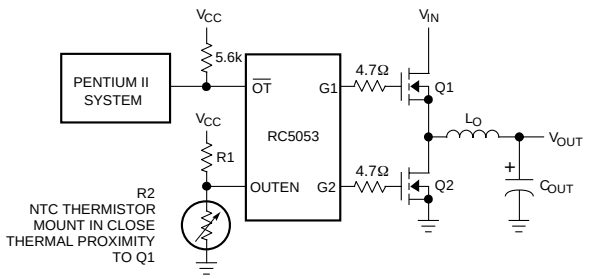


Figure 6. OUTEN Pin as a Thermistor Input

Clock Synchronization

The internal oscillator can be synchronized to an external clock by applying the external clocking signal to the OUTEN pin. The synchronizing range extends from the initial operating frequency up to 500kHz. If the external frequency is much higher than the natural free-running frequency, the peak-to-peak sawtooth amplitude within the RC5053 will decrease. Since the loop gain is inversely proportional to the amplitude of the sawtooth, the compensation network may need to be adjusted slightly. Note that the temperature sensing circuitry does not operate when external synchronization is used.

MOSFET Gate Drive

Power for the internal MOSFET drivers is supplied by PV_{CC}. This supply must be above the input supply voltage by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 7. The 82% typical maximum duty cycle ensures sufficient off-time to refresh the charge pump during each cycle.

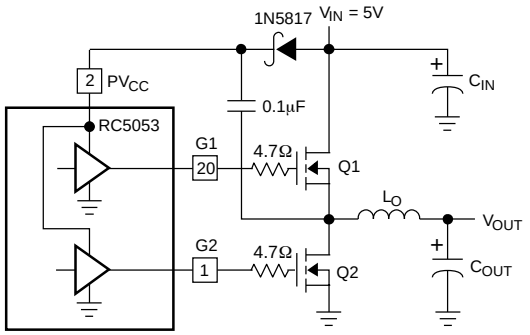


Figure 7. Doubling Charge Pump

Upon power-down, G1 and G2 will both be held low to prevent output voltage under shoot. On power-up or wake-up from thermal shutdown, the driver is designed such G2 will be held low until after G1 first goes high.

Power MOSFETs

Two N-channel power MOSFETs are required for most RC5053 circuits. They should be selected based primarily on gate threshold and on-resistance considerations. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate driver charge pump scheme. In 5V input designs where a 12V supply is used to power PV_{CC}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. However, logic level devices will improve efficiency. The current drawn from the 12V supply varies with the MOSFETs used and the RC5053 operating frequency, but is generally less than 50mA.

RC5053 designs that use a 5V V_{IN} voltage and a doubler charge pump to generate PV_{CC} will not provide enough drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the MOSFETs and reducing efficiency. Logic level MOSFETs are a better choice for 5V-only systems. They can be fully enhanced with the generated charge pump voltage and will operate at maximum efficiency. See the MOSFET Gate Drive section for more charge pump information.

Once the threshold voltage has been selected, $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical RC5053 buck converter circuit the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2 R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{[DC(Q1)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q1)}]}{(V_{OUT})(I_{MAX})^2}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{[DC(Q2)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q2)}]}{(V_{IN} - V_{OUT})(I_{MAX})^2}$$

P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A typical high efficiency circuit designed for Pentium II with a 5V input and a 2.0V, 14.2A output might allow no more than 4% loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

[(2.0)(14.2A/0.9)(0.04)] = 1.26W per MOSFET
and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{(5V)(1.26W)}{(2.0V)(14.2A)^2} = 0.016\Omega$$

$$R_{DS(ON)Q2} = \frac{(5V)(1.26W)}{(5V - 2.0V)(14.2A)^2} = 0.010\Omega$$

Note also that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the dissipation numbers are only 1.26W per device or less—large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Fairchild NDB6030L are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of gate drive that work well in RC5053 circuits. With lower output voltages, the $R_{DS(ON)}$ of Q2 may need to be significantly lower than that for Q1. These conditions can often be met by paralleling two MOSFETs for Q2 and using a single device for Q1. Note that using a higher P_{MAX} value in the $R_{DS(ON)}$ calculations will generally decrease MOSFET cost and circuit efficiency while increasing MOSFET heat sink requirements.

Inductor Selection

The inductor is often the largest component in the RC5053 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements, output ripple requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the RC5053. In a typical 5V input, 2.0V output application, the maximum current slew rate will be:

$$DC_{MAX}\frac{(V_{IN} - V_{OUT})}{L} = \frac{2.46}{L} \quad \frac{A}{\mu s}$$

where L is the inductor value in μH. With proper frequency compensation, the combination of the inductor and output capacitor will determine the transient recovery time. In general, a smaller value inductor will improve transient response at the expense of increased output ripple voltage and inductor core saturation rating. A 2μH inductor would have a 1.23A/μs rise time in this application, resulting in a 4.1μs delay in responding to a 5A load current step. During this 4.1μs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1μH to 5μH range for most typical 5V input RC5053 circuits. To optimize performance, different combinations of input and output voltages and expected loads may require different inductor values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to- peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = RC5053 oscillator frequency = 300kHz
L_O = Inductor value

Solving this equation with our typical 5V to 2.0V application with a 2μH inductor, we get:

$$\frac{(3.0)(0.40)}{(300kHz)(2\mu H)} = 2A_{p\text{-}p}$$

Peak inductor current at 14.2A load:

$$14.2A + \frac{2A}{2} = 15.2A$$

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in noncurrent limited circuits, the current in the inductor may rise above this maximum under short circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

Input and Output Capacitors

A typical RC5053 design puts significant demands on both the input and the output capacitors. During constant load operation, a buck converter like the RC5053 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 peak-to-peak ripple current, and the minimum value is zero. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation.

Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (three months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature will have the largest effect on capacitor longevity.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the RC5053 can adjust the inductor current to the new value. Output capacitor ESR results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 11A load step with a 0.05Ω ESR output capacitor will result in a 550mV output voltage shift; this is 27.5% of the output voltage for a 2.0V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in RC5053 applications. OS-CON electrolytic capacitors from SANYO and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular surge tested tantalum capacitors that work well in RC5053 applications.

A common way to lower ESR and raise ripple current is to parallel several capacitors. A typical RC5053 application might exhibit 5A input ripple current. SANYO OS-CON part number 10SA220M (220μF/10V) capacitors feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) will meet the above requirements. Similarly, AVX TPSE337M006R0100 (330μF/6V) have a rated maximum ESR of 0.1Ω; seven in parallel will lower the net output capacitor ESR to 0.014Ω. For low cost application, SANYO MV-GX series of capacitors can be used with acceptable performance.

Feedback Loop Compensation

The RC5053 voltage feedback loop is compensated at the COMP pin, attached to the output node of the internal gm error amplifier. The feedback loop can generally be compensated properly with an RC + C network from COMP to GND as shown in Figure 8.

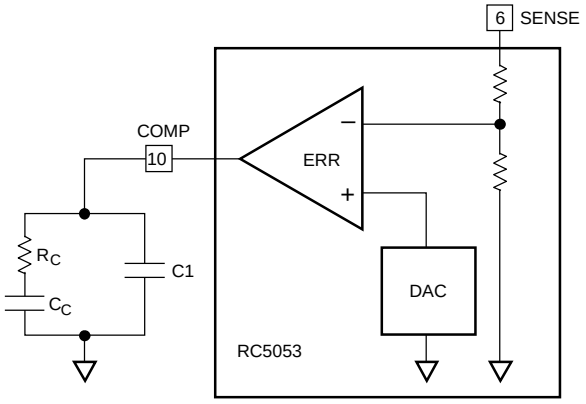


Figure 8. Compensation Pin Hook-Up

Loop stability is affected by the inductor and output capacitor values and by other factors. Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting a transient

current at the load and using an RC network box to iterate toward the final compensation values, or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

Table 4. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 330µF AVX TPS Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (pF)	C1 (pF)
1	990	3.6	10000	470
1	1980	6.8	4700	220
1	4950	22	2200	100
2.7	990	10	3300	150
2.7	1980	20	2200	68
2.7	4950	51	1000	47
5.6	990	20	2200	68
5.6	1980	39	1000	47
5.6	4950	100	470	33

Table 4 shows the suggested compensation components for 5V input applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors as the output capacitor. The optimum component values might deviate from the suggested values slightly because of board layout and operating condition differences.

An alternate output capacitor is the Sanyo MV-GX series. Using multiple parallel 1500µF Sanyo MV-GX capacitors for the output capacitor, Table 5 shows the suggested compensation component value for a 5V input application based on the inductor and output capacitor values.

Table 5. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 1500µF SANYO MV-GX Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (pF)	C1 (pF)
1	4500	9.1	3300	150
1	6000	10	3300	100
1	9000	18	2200	68
2.7	4500	22	1500	47
2.7	6000	30	1000	47
2.7	9000	47	680	33
5.6	4500	47	680	33
5.6	6000	62	470	33
5.6	9000	91	330	22

VID0 to VID4, PWRGD and $\overline{\text{FAULT}}$

The digital inputs (VID0 to VID4) program the internal DAC which in turn controls the output voltage. These digital input controls are intended to be static and are not designed for high speed switching. Forcing V_{OUT} to step from a high to a low voltage by changing the VID_n pins quickly can cause $\overline{\text{FAULT}}$ to trip.

Figure 9 shows the relationship between the V_{OUT} voltage, PWRGD and $\overline{\text{FAULT}}$. To prevent PWRGD from interrupting the CPU unnecessarily, the RC5053 has a built-in t_{PWRBAD} delay to prevent noise at the SENSE pin from toggling PWRGD. The internal time delay is designed to take about 500µs for PWRGD to go low and 1ms for it to recover. Once PWRGD goes low, the internal circuitry watches for the output voltage to exceed 115% of the rated voltage. If this happens, $\overline{\text{FAULT}}$ will be triggered. Once $\overline{\text{FAULT}}$ is triggered, G1 and G2 will be forced low immediately and the RC5053 will remain in this state until V_{CC} power supply is recycled or OUTEN is toggled.

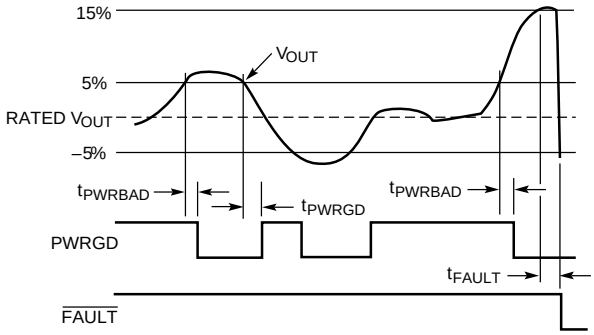


Figure 9. PWRGD and $\overline{\text{FAULT}}$

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RC5053. These items are also illustrated graphically in the layout diagram of Figure 10. The thicker lines show the high current paths. Note that at 10A current levels or above, current density in the PC board itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz copper requires a minimum trace width of 0.15" to carry 10A.

1. In general, layout should begin with the location of the power devices. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find

Preliminary Information

routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.

2. The GND and SGND pins should be shorted right at the RC5053. This helps to minimize internal ground disturbances in the RC5053 and prevents differences in ground potential from disrupting internal circuit operation. This connection should then tie into the ground plane at a single point, preferably at a fairly quiet point in the circuit such as close to the output capacitors. This is not always practical, however, due to physical constraints. Another reasonably good point to make this connection is between the output capacitors and the source connection of the lowside FET Q2. Do not tie this single point ground in the trace run between the low side FET source and the input capacitor ground, as this area of the ground plane will be very noisy.

3. The small signal resistors and capacitors for frequency compensation and soft start should be located very close to their respective pins and the ground ends connected to the signal ground pin through a separate trace. Do not connect these parts to the ground plane!

4. The V_{CC} and PV_{CC} decoupling capacitors should be as close to the RC5053 as possible. The 10µF bypass capacitors for V_{CC} and a 1µF bypass capacitor for PV_{CC} will help provide optimum regulation performance.

5. The (+) plate of C_{IN} should be connected as close as possible to the drain of the upper MOSFET. An additional 1µF ceramic capacitor between V_{IN} and power ground is recommended.

6. The SENSE pin is very sensitive to pickup from the switching node. Care should be taken to isolate SENSE from possible capacitive coupling to the inductor switching signal. A 0.1µF is required between the SENSE pin and the SGND pin next to the RC5053.

7. OUTEN is a high impedance input and should be externally pulled up to a logic HIGH for normal operation.

8. Kelvin sense I_{MAX} and I_{FB} at Q1 drain and source pins.

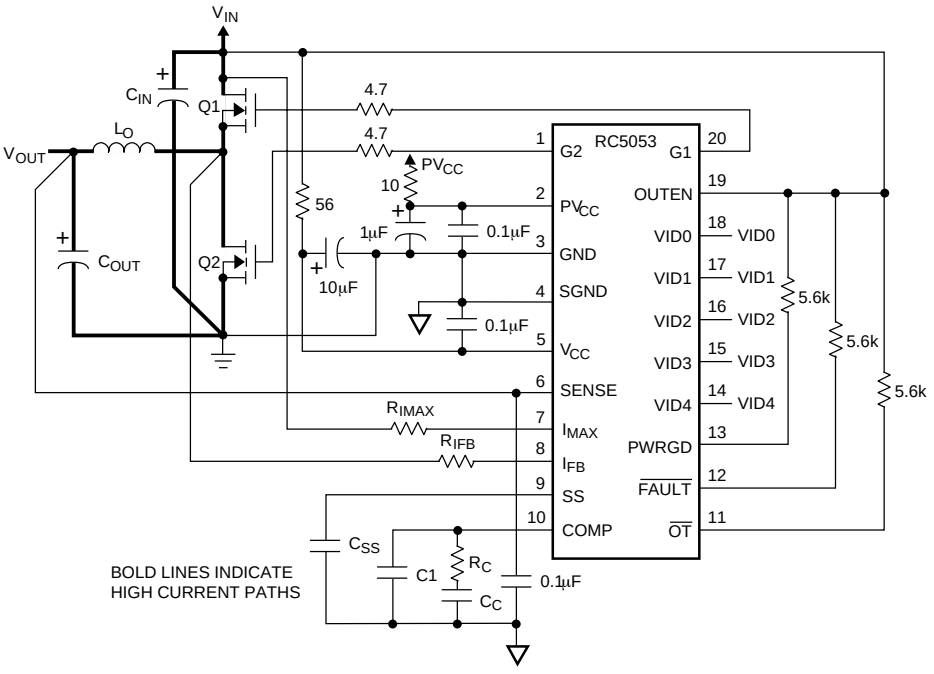


Figure 10. RC5053 Layout Diagram

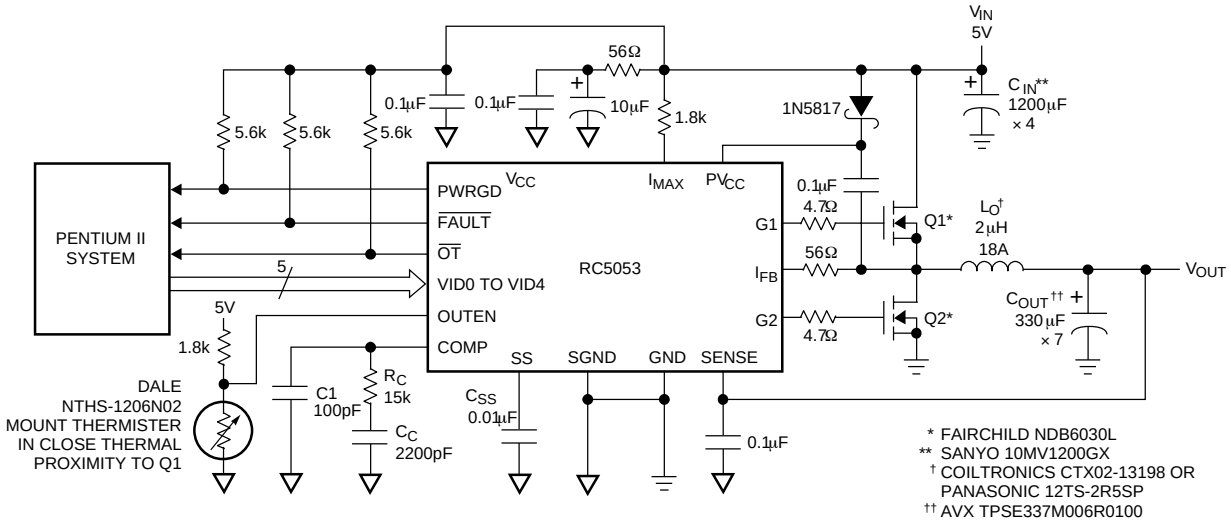


Figure 11. Single Supply RC5053 5V to 1.8V-3.5V Application with Thermal Monitor

Preliminary Information

Notes:

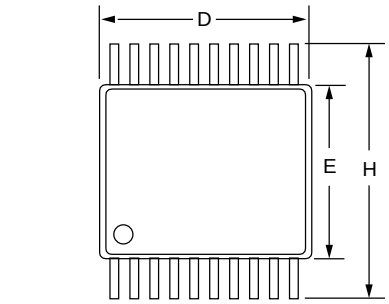
Notes:

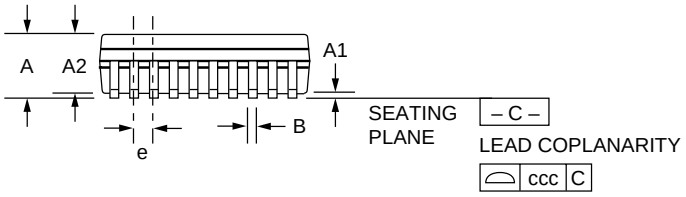
Mechanical Dimensions (20 Lead SSOP)

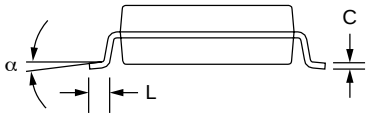
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.079	—	2.00	
A1	.002	—	0.05	—	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	5
c	.004	.010	0.09	0.25	5
D	.272	.295	6.90	7.50	2, 4
E	.291	.323	7.40	8.20	
E1	.197	.220	5.00	5.60	2
e	.026 BSC		0.65 BSC		
L	.022	.037	0.55	0.95	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







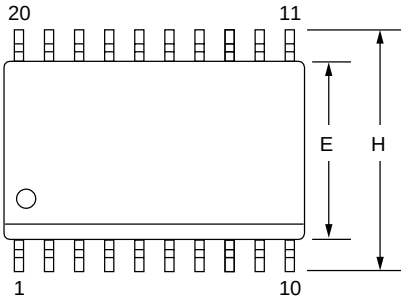
Preliminary Information

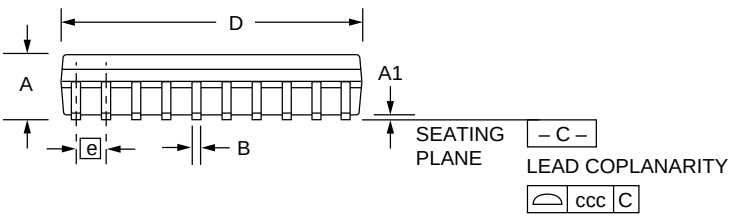
Mechanical Dimensions (20 Lead SOIC)

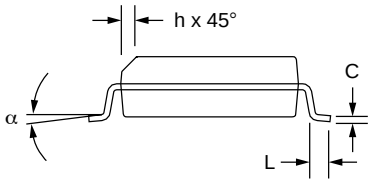
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5053M	SOIC
RC5053F	SSOP